TWO MARK QUESTIONS-ANSWERS

Unit – 1

BASIC CONCEPTS

1. Define binary logic? [May 2017]

Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

2. What are the basic digital logic gates? [Nov 2017]

The three basic logic gates are

- AND gate
- OR gate
- NOT gate

3. What is a Logic gate? [May 2016]

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

4. Which gates are called as the universal gates? What are its advantages? [May 2015]

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

5. What are basic properties of Boolean algebra? [May 2014]

The basic properties of Boolean algebra are commutative property, associative Property and distributive property.

6. State the associative property of boolean algebra. [Nov 2017]

The associative property of Boolean algebra states that the OR ing of several variables results in the same regardless of the grouping of the variables. The associative property is stated as follows:

A+ (B+C) = (A+B) +C

7. State the commutative property of Boolean algebra. [Nov 2016]

The commutative property states that the order in which the variables are OR ed makes no difference. The commutative property is:

A+B=B+A

8. State the distributive property of Boolean algebra. [Nov 2015]

The distributive property states that AND ing several variables and OR ing the result With a single variable is equivalent to OR ing the single variable with each of the the several Variables and then AND ing the sums. The distributive property is: A+BC= (A+B) (A+C)

9. State the absorption law of Boolean algebra. [Nov 2014]

The absorption law of Boolean algebra is given by X+XY=X, X(X+Y) =X.

10. State De Morgan's theorem. [Nov 2013]

De Morgan suggested two theorems that form important part of Boolean algebra.

They are,

The complement of a product is equal to the sum of the complements. (AB)' = A' + B'

The complement of a sum term is equal to the product of the complements. (A + B)' = A'B'

11. Reduce A (A + B) [May 2014]

A (A + B) = AA + AB

= A (1 + B) [1 + B = 1]

= A.

12. Reduce A'B'C' + A'BC' + A'BC[May 2015]

A'B'C' + A'BC' + A'BC = A'C'(B' + B) + A'B'C

= A'C' + A'BC [A + A' = 1]

= A'(C' + BC)

= A'(C' + B) [A + A'B = A + B]

Unit–2

COMBINATIONAL LOGIC CIRCUITS

1. Define combinational logic[May 2014]

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

2. Explain the design procedure for combinational circuits[May 2017]

- The problem definition
- Determine the number of available input variables & required O/P variables.
- Assigning letter symbols to I/O variables
- Obtain simplified Boolean expression for each O/P.
- Obtain the logic diagram.
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3. Define Half adder and full adder[May 2015]

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

4. Define Decoder? [Nov 2013]

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

5. What is binary decoder? [Nov 2016]

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

4. Define Encoder? [May 2016]

An encoder has 2ninput lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

5. What is priority Encoder? [Nov 2014]

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

6. Define multiplexer? [May 2014]

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

7. What do you mean by comparator[May 2012]

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

Unit 3

SYNCHRONOUS SEQUENTIAL CIRCUITS

1. What are the classification of sequential circuits? [Nov **2017]**

The sequential circuits are classified on the basis of timing of their signals into two types. They are,

- Synchronous sequential circuit.
- Asynchronous sequential circuit.
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2. Define Flip flop. [May 2014]

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3.What are the different types of flip-flop? [Nov 2015]

There are various types of flip flops. Some of them are mentioned below they are,

- RS flip-flop
- SR flip-flop
- D flip-flop
- JK flip-flop
- T flip-flop

4.What is the operation of D flip-flop? [May 2016]

In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

5. What is the operation of JK flip-flop? [Nov 2016]

•When K input is low and J input is high the Q output of flip-flop is set.
•When K input is high and J input is low the Q output of flip-flop is reset.
•When both the inputs K and J are low the output does not change
•When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.

6. What is the operation of T flip-flop? [May 2017]

T flip-flop is also known as Toggle flip-flop.
•When T=0 there is no change in the output.
•When T=1 the output switch to the complement state (ie) the output toggles.

7. Define race around condition. [Nov 2013]

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

8. What is edge-triggered flip-flop? [May 2015]

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

9. What is a master-slave flip-flop? [Nov 2014]

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

10. Define rise time. [May 2013]

The time required to change the voltage level from 10% to 90% is known as rise time (tr).

11. Define fall time. [Nov 2012]

The time required to change the voltage level from90% to 10% is known as fall time (tf).

12. Define skew and clock skew. [May 2014]

The phase shift between the rectangular clock wave forms is referred to as skew and the time delay between the two clock pulses is called clock skew.

13. Define setup time. [Nov 2011]

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t set up.

14. Define hold time. [May 2017]

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as t_{hold} .

15. Define propagation delay. [Nov 2013]

A propagation delay is the time required to change the output after the application of the input.

16. Define registers. [May 2010]

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

17. Define shift registers. [Nov 2016]

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

18. What are the different types of shift type? [May 2011]

There are five types. They are,

- Serial In Serial Out Shift Register
- Serial In Parallel Out Shift Register
- Parallel In Serial Out Shift Register
- Parallel In Parallel Out Shift Register
- Bidirectional Shift Register

19. Define sequential circuit? [Nov 2010]

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

20. What do you mean by present state? [May 2013]

The information stored in the memory elements at any given time defines the present state of the sequential circuit.

21. What do you mean by next state? [Nov 2012]

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

22. State the types of sequential circuits? [May 2016]

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

23. Define synchronous sequential circuit[Nov 2015]

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

Unit 4

ASYNCHRONOUS SEQUENTIAL CIRCUITS

1. Define Asynchronous sequential circuit? [May 2016]

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

2. What is race around condition? [Nov 2015]

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

3. The t pd for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter[May 2017]

f max (ripple) = 5 x 50 ns = 4 MHZ

4. What are secondary variables? [Nov 2017]

Present state variables in asynchronous sequential circuits

5. **What are excitation variables? [May 2015]**

Next state variables in asynchronous sequential circuits

6. **What is fundamental mode sequential circuit? [Nov 2014]**

- -input variables changes if the circuit is stable
- -inputs are levels, not pulses
- -only one input can change at a given time

7. **What are pulse mode circuit? [May 2013]**

- -inputs are pulses
- -width of pulses are long for circuit to respond to the input
- -pulse width must not be so long that it is still present after the new state is reached

8. **What are the significance of state assignment? [Nov 2013]**

In synchronous circuits-state assignments are made with the objective of circuit reduction Asynchronous circuits-its objective is to avoid critical races

9. **When do race condition occur? [May 2012]**

Two or more binary state variables change their value in response to the change in i/p variable

10. **What is non critical race? [Nov 2012]**

- -final stable state does not depend on the order in which the state variable changes
- -race condition is not harmful

11. **What is critical race? [May 2013]**

- -final stable state depends on the order in which the state variable changes
- -race condition is harmful

12. **When does a cycle occur? [Nov 2016]**

Asynchronous circuit makes a transition through a series of unstable state

13. **What are the different techniques used in state assignment? [May 2014]**

- -shared row state assignment
- -one hot state assignment
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14. **What are the steps for the design of asynchronous sequential circuit? [Nov 2017]**

- -construction of primitive flow table
- -reduction of flow table
- -state assignment is made
- -realization of primitive flow table

15. **What is hazard? [May 2012]**

Unwanted switching transients is Called hazards

16. What is static 1 hazard? [Nov 2011]

Output goes momentarily 0 when it should remain at 1

17. What is static 0 hazard? [May 2011]

Output goes momentarily 1 when it should remain a t 0

18. What is dynamic hazard? [Nov 2017]

Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

19. What is the cause for essential hazards? [May 2016]

Unequal delays along 2 or more path from same input

20. What is flow table and primitive flow chart? [Nov 2013]

State table of ansynchronous sequential network .primitive flow chart is one stable state per row

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21. Define merger graph. [May 2015]

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. It two states are incompatible no connecting line is drawn.

22. Define closed covering[Nov 2014]

A Set of compatibles is said to be closed if, for every compatible contained in the set, all its implied compatibles are also contained in the set. A closed set of compatibles, which contains all the states of M, is called a closed covering.

23. Define state table. [May 2014]

For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

24. Define total state[Nov 2016]

The combination of level signals that appear at the inputs and the outputs of the delays define what is called the total state of the circuit.

25. What are the steps for the design of asynchronous sequential circuit? [May 2010]

1. Construction of a primitive flow table from the problem statement.
2. Primitive flow table is reduced by eliminating redundant states using the state reduction
3. State assignment is made
4. The primitive flow table is realized using appropriate logic elements.

Unit 5

LOGIC FAMILIES AND PROGRAMMABLE LOGIC DEVICES

1. Mention the important characteristics of digital IC's? [Nov 2015]

- Fan out
- Power dissipation
- Propagation Delay
- Noise Margin
- Fan In
- Operating temperature
- Power supply requirements

2. List basic types of programmable logic devices. [May 2016]

- . Read only memory
- . Programmable logic Array
- . Programmable Array Logic
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3. Explain ROM[Nov 2017]

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is 2n.

4. Define address and word: [May 2015]

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

5. State the types of ROM[Nov 2016]

- . Masked ROM.
- . Programmable Read only Memory
- . Erasable Programmable Read only memory.
- . Electrically Erasable Programmable Read only Memory.
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6. What is programmable logic array? How it differs from ROM? [May 2014]

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA.A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

7. Explain PROM. [Nov 2013]

PROM (Programmable Read Only Memory) It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

8. Explain EPROM. [May 2017]

EPROM (Erasable Programmable Read Only Memory) EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

9. Explain EEPROM. [Nov 2012]

EEPROM (Electrically Erasable Programmable Read Only Memory) EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

10. What is RAM? [May 2013]

Random Access Memory. Read and write operations can be carried out.

11. What is programmable logic array? How it differs from ROM? [Nov 2015]

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA.A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the minterms as in the ROM.

12. What is mask - programmable? [May 2012]

With a mask programmable PLA, the user must sub mita PLA program table to the manufacturer.

13. What is field programmable logic array? [Nov 2010]

The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the EPLA.

14. List the major differences between PLA and PAL[May 2015]

PLA

Both AND and OR arrays are programmable and Complex .Costlier than PAL AND

PAL

arrays are programmable OR arrays are fixed .Cheaper and Simpler

15. Define PLD. [Nov 2017]

Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.

16. Give the classification of PLDs. [May 2016]

PLDs are classified as PROM (Programmable Read Only Memory), Programmable Logic Array(PLA), Programmable Array Logic (PAL), and Generic Array Logic(GAL)

17. Define PROM. [Nov 2013]

PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.

18. Define PLA[May 2014]

PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.

19. Define PAL[Nov 2012]

PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

20. Why was PAL developed ? [May 2015]

It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

21. Why the input variables to a PAL are buffered? [Nov 2014]

The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.

22. What does PAL 10L8 specify? [May 2011]

PAL - Programmable Logic Array 10 - Ten inputs L - Active LOW Output 8 - Eight Outputs

PART-B

UNIT 1

1. **(i) Express the Boolean function F = A+B'C in a sum of minterms. (6)**
   (ii) Simplify the following Boolean function using K-map (10)
   F(w,x,y,z) = ∑m(0, 1,2,4,5,6,8,9,12,13,14) [May 2017]
2. **(i) Simplify the following Boolean function using Quine – McCluskey method.**
   F(A,B,C,D) = ∑m(0, 2,3,6,7,8,10,12,13) (8)
   (ii) Draw the schematic and explain the operation of a CMOS inverter. Also explain its characteristics. (8) [May 2016]
3. **(i) Simplify the following Boolean function using 4 – Variable map**
   F(w,x,y,z) = ∑m(2,3,10,11,12,13,14,15) (8)
   (ii) Draw a NAND logic diagram that implements the complement of the following function.
   F(A,B,C,D) = ∑m(0,1,2,3,4,8,9,12) (8) [Dec 2016]
4. **Using QM method simplify the Boolean expression**
   f(x1,x2,x3,x4,x5) = ∑(0,1,4,5,16,17,21,25,29) [Dec 2015]
5. **(i) Express the following Boolean function as POS and SOP form. D = (A'+B)(B'+C) (4)**
   (ii) Minimise using Quine Mc-Clusky and verify using k-map methods.
   M(0,1,4,11,13,15) +d(5,7,8) (12) [May 2014]
6. **Implement the following using NOR gates.**
   output = 1, when the inputs are m(0,1,2,3,4)
   =0, when the inputs are m(5,6,7) (8) [May 2015]
7. **i) Express the Boolean function F=XY + X' Z in product of Maxterm. (6) [Nov-2017]**
   ii) Reduce the following function using K-map technique (10)
   f (A,B,C,D) = Π□ (0,3,4,7,8,10,12,14)+d (2, 6)
8. **Simplify the following Boolean function F together with don't care condition using Karnaugh map method.**
   a. **F(A,B,C,D) = ∑m(0, 6, 8, 13,14), d(A, B, C, D) = ∑m(2, 4, 10)**
   b. **F(A,B,C,D) = ∑m(0, 2, 4, 5, 8, 14, 15), d(A, B, C, D) = ∑m(7, 10,13)**
   c. **F(A,B,C,D) = ∑m(4, 6, 7, 8, 12, 15), d(A, B, C, D) =∑m(2,3,5,10,11,14) [May 2016]**
9. **Simplify the following Boolean expressions to a minimum number of literals.**
   (i) $\underline{A}BC + AB\overline{C} + \overline{A}B$
   (ii) $A\underline{BC} + \underline{A}C + \overline{B}$
   (iii)$(A+B)(A+\underline{B})$
   (iv)$BC(\underline{A}D + \underline{A}D) + A\overline{B}$
   (v) (A + B+ AB)(AB + AC + BC) [May 2009]
10. **(i) Obtain the canonical POS for F(A,B,C,D) = (A+B')(B+C)(A+C')**
    (ii) Using k-map method obtain the minimal SOP and POS expressions for the function F(x,y,z,w) = ∑(1,3,4,5,6,7,9,12,13) [Dec 2015]

UNIT 2

1. **(i) Design a full adder using two half adders and an OR gate. (6)**
   (ii) Explain the operation of a BCD adder. (10) [May 2017]
2. **(i) Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation. (8)**
   (ii) Implement the following function using suitable multiplexer
   $F(A, B, C, D) = \sum (1, 3, 4, 11, 12, 13, 14, 15)$ (8) [May 2017]
3. **(i) Design a combinational circuit that generates the 9's complement of a BCD digit (8)**
   (ii) Explain the operation of carry lookahead adder with neat diagram. (8) [Dec 2016]
4. **(i) Define fan-in, fan-out and Noise margin. (6)**
   (ii) Design a combinational system that produces the product of 2 binary number A=(A1,A0) X B=(B2,B1,B0) (10) [Dec 2015]
5. **(i) Derive the equation for a 4-bit look ahead carry adder circuit. (6)**
   (ii) Draw and explain the block diagram of a 4-bit serial adder to add the contents of two registers.
   (10) [May 2016]
6. **(i) Multiply (1011)2 by (1101)2 using addition and shifting operation. also draw block diagram of the 4-bit by 4-bit parallel multiplier. (8)**
   (ii) Design and implement the conversion circuits for binary code to gray code. (8) [May 2014]
7. **A) Design a carry look ahead adder with necessary diagrams.(16) [Nov-2015]**
   B) i) Implement full subtractor using demultiplexer.(10) [Nov-2014]
   ii) Implement the given boolean expression using 8:1 multiplexer (6) [Nov-2010]
   $F(A, B, C) = \sum (1, 3, 5, 6)$

UNIT 3

1. (i) **Covert D to T flip flop. (6)**
   (ii) Design a serial binary adder. (10) [May 2016]
2. **(i) Explain the operation of a BCD ripple counter with JK flipflops. (8)**
   (ii) Design a clocked sequential machine using T flip-flops for the following state diagram . (use straight binary assignment).(8) [May 2017]
3. **(i) Provide the characteristic table, characteristic equation and excitation table of D flip-flop and JK flip- flop. (6)**
   (ii) Explain the operation of universal shift register with neat block diagram. (10) [Nov 2016]
4. **With a neat state diagram and logic diagram, design and explain the sequence of states of BCD counter. (16) [Nov 2017]**
5. **(i) Construct a clocked JK flip flop which is triggered at the positive edge of the clock pulse from a clocked SR flip flop consisting of NOR gates. (4) [Nov 2015]**

   (ii)Design a synchronous up/down counter that will count up from zero to one to two to three and will repeat whenever an external input x is logic 0, and will count down from three to two to one to zero and will repeat whenever the external input x is logic 1. Implement your circuit with one TTL SN74LS76 device and one TTL SN74LS00 device. (12) [May 2016]

6. **(i) Write down the characteristic table for the JKflip flop with NOR gates. (4)**
   (ii) What is meant by USR? Explain the principle of operation of 4-bit USR. (12) [May 2014]

UNIT 4

1. **Draw the ASM chart for the following state diagram.(8) [May 2017]**
(ii) Design the following synchronous sequential circuit using D flip flop and logic gates. (8) [May 2016]

2. What is an Hazard? What are the types of hazards? Check whether the following circuit contains an hazard or not Y = x1x2 + x2'x3. If th hazard is present, demonstrate its removal. [May 2015]

3. For the state diagram shown in fig. (1), design a synchronous sequential circuit using JK flip-flop. [Dec 2016]

4. (i) Differentiate critical races from non-critical races. (6)
(ii) Explain the steps involved in the reduction of state table. (10) [Dec 2017]

5. For the circuit shown in figure, write down the state table and draw the state diagram and analyze the operation. [May 2016]

6. What are essential hazards? How does the hazard occur in sequential circuits? How can the same be eliminated using SR latches? Give an example. [May 2014]

7.Design a three bit binary counter using T flipflops. [Nov-2013]

8.Design an asynchronous sequential circuit wih inpus x1 and x2 and one output z. Initially both the inputs are equal to 0. When x1 and x2 becomes 1, z becomes 1. When second input also becomes 1, z = 0; The output stays at 0 until circuit goes back to initial state. [May 2016]

9. Discuss in detail the static hazards. [May 2009]
10. a) Develop the state diagram and primitive flow table for a logic system that has 2 inputs, x and y and an output z. And reduce primitive flow table. The behavior of the circuit is stated as follows. Initially x = y = 0. Whenever x = 1 and y = 0 then z = 1, whenever x = 0 and y = 1 then z = 0. When x = y = 0 or x = y = 1 no change in z it remains in the previous state. The logic system has edge-triggered inputs without having a clock. The logic system changes state on the rising edges of the 2 inputs. Static input values are not to have any effect in changing the z output. [May 17/ Dec 10]

UNIT 5

1. (i) Deign a combinational circuit using a ROM.The circuit accepts a three bit number and outputs a binary number equal to the square of the input number. (10)

(ii) Explain briefly EPROM and EEPROM technology. (6) [May 2017]

2. (i) Implement the following functions using 3 input, 4 product term and 2 output PLA.

F1 = AB' + AC + A'BC'

F2 = (AC + BC)' (8)

(ii) With logic diagram, explain the basic macrocell. (8) [May 2016]

3. (i) Explain read and write operation of memory with timing waveforms. (8)

(ii) Write a note on RAM. (8) [Nov 2015]

4. (i) Draw a PLA circuit to implement the functions (8)

***F* 1= □*A* ' *B*+ □□*AC* '+ *A*' *BC* '; *F* 2=(□□*AC*+ □□*AB*+ □□*BC*□□) '.**

(ii) Write a note on FPGA. (8) [Nov 2017]

5. (i) We can expand the word size of a RAM by combining two or more RAM chips. For instance, we can use two 32X8 memory chips where he number 32 represents the number of words and 8 represents the umber of bits per word, to obtain a 32X16 RAM. In this case the number of words remains the same but the length of each word will two bytes long. Draw a block diagram to show how we can use two 16X4 memory chips to obtain a 16X8 RAM. (8)

(ii) Explain the principle of operation of Bipolar SRAM cell. (8) [May 2014]

6. (i) A combinational circuit is defined as the functions

F1=AB'C' + AB'C + ABC

F2= A'BC + AB'C + ABC

Implement the digital circuit with a PLA having 3 inputs, 3 product terms, and 2 outputs. (8)

(ii) Write a note on SRAM based FPGA. (8) [May 2015]

7.Implement the following Boolean function with a PLA. (16) [Nov-2014]

$$F_1(A, B, C) = \sum (0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum (0, 5, 6, 7)$$

$$F_3(A, B, C) = \sum (0, 3, 5, 7)$$